WHAT IS CLAIMED IS:

1. A pixel-data processing arrangement, comprising:

a vertical processing circuit including a polyphase filter and a line-buffer circuit, the vertical processing circuit adapted to receive and circulate pixel data and through the line-buffer circuit and from the line-buffer circuit to the polyphase filter, the polyphase filter being adapted to filter the pixel data and perform peaking and scaling functions concurrently by using a first set of coefficients, the first set of coefficients resulting from a convolution of peaking filter coefficients with scaling filter coefficients; and

a logic circuit adapted to cause the vertical processing circuit to operate in the first operational mode in which the filtered data is processed by using the first set of coefficients and circulating the filtered data through the line-buffer circuit and to switch between the first operational mode and a second operational mode in which the vertical processing circuit performs another function by using a set of coefficients that is different than the first set of coefficients.

2. The pixel-data processing arrangement of claim 1, further including a storage unit adapted to receive and store processed pixel data, and wherein in the first operational mode the vertical processing circuit receives the pixel data at a first rate and outputs the processed pixel data for storage in the storage unit at a second pixel rate, the second pixel rate being different than the first pixel rate.

3. The pixel-data processing arrangement of claim 2, wherein the first pixel rate is faster than the second pixel rate.

4. The pixel-data processing arrangement of claim 2, wherein the first pixel rate is two pixels per cycle and the second pixel rate is one pixel per cycle.

5. The pixel-data processing arrangement of claim 1, wherein the other function performed by the vertical processing circuit is an N-taps scaling function, where N is an integer greater than 2.

6. The pixel-data processing arrangement of claim 1, wherein the other function performed by the vertical processing circuit is an N-taps averaging-filter function in which pixels neighboring a current pixel are averaged and where N is an integer greater than 2.

7. The pixel-data processing arrangement of claim 1, wherein the first set of coefficients results from a convolution of 3 taps of peaking filter coefficients with 4 taps of scaling filter coefficients.

8. The pixel-data processing arrangement of claim 1, wherein the vertical processing circuit and the logic circuit are implemented using a programmed processor.

9. The pixel-data processing circuit of claim 1, wherein the logic circuit is implemented using a programmed processor.

10. A pixel-data processing arrangement, comprising:

vertical processing means including line-buffer means for buffering lines of pixel data and polyphase filter means for polyphase filtering pixel data received from the line-buffer means, the vertical processing means for receiving and circulate pixel data and through the line-buffer means and from the line-buffer means to the polyphase filter means, the polyphase filter means also for performing peaking and scaling functions concurrently by using a first set of coefficients, the first set of coefficients resulting from a convolution of peaking filter coefficients with scaling filter coefficients; and

a logic circuit adapted to cause the vertical processing means to operate in the first operational mode in which the filtered data is processed by using the first set of coefficients and circulating the filtered data through the line-buffer means and to switch between the first

operational mode and a second operational mode in which the vertical processing means performs another function by using a set of coefficients that is different than the first set of coefficients.

11. A method for pixel-data processing, comprising:

vertical processing pixel-data including

buffering lines of pixel data and, in response,

polyphase filtering buffered pixel data,

receiving and circulating the pixel data for further buffering, and the polyphase filtering including peaking and scaling functions concurrently by using a first set of coefficients, the first set of coefficients resulting from a convolution of peaking filter coefficients with scaling filter coefficients; and

causing the vertical processing to operate in the first operational mode in which the filtered data is processed by using the first set of coefficients and circulating the filtered data, and to switch between the first operational mode and a second operational mode in which the vertical processing includes performing another function by using a set of coefficients that is different than the first set of coefficients.

12. The method of claim 11, wherein the other function is an N-taps scaling function, where N is an integer greater than 2.

13. The method of claim 11, wherein the first set of coefficients results from a convolution of M taps of peaking filter coefficients with N taps of scaling filter coefficients, and further including selecting the other function as one of: an N-taps scaling function, and an N-taps averaging-filter function in which pixels neighboring a current pixel are averaged, where each of M and N is an integer greater than 2.

14. A pixel-data processing arrangement, comprising:

storage means for receiving and storing processed pixel data;

processing means for processing pixel data, the processing means including a vertical processing means including a polyphase filter and a line-buffer circuit, the vertical processing means having a first operational mode in which pixel data is received at a first pixel rate and circulated through the line-buffer circuit, the circulated data being manipulated by the vertical processing means, and the vertical processing means being configured to perform a first function using a first set of operating coefficients, and the processed pixel data is output for storage in the storage means at a second pixel rate, the second pixel rate being different than the first pixel rate; and

means for causing the processing means to switch between the first operational mode and one of at least two other selectable operational modes, each of the at least two other selectable operational modes including circulating data for processing by the vertical processing means, wherein the first set of operating coefficients are pre-determined from a convolution of a second set of operating coefficients defining a second data-manipulation function and a third set of operating coefficients defining a third data-manipulation function, and the first function providing a result that is the same as a result that would be provided by the second and third functions being performed cascaded.

15. The pixel-data processing arrangement of claim 14, wherein the first pixel rate is faster than the second pixel rate.

16. The pixel-data processing arrangement of claim 14, wherein the first pixel rate is two pixels per cycle and the second pixel rate is one pixel per cycle.

17. The pixel-data processing arrangement of claim 14, wherein said at least two other selectable operational modes includes a function performed by the vertical processing circuit using an N-taps scaling function, where N is an integer greater than 2.

18. The pixel-data processing arrangement of claim 14, wherein said at least two other selectable operational modes includes a function performed by the vertical processing circuit

using an N-taps scaling function, includes another function performed by the vertical processing circuit using an M-taps averaging-filter function in which pixels neighboring a current pixel are averaged, and where each of M and N is an integer greater than 2.

19. The pixel-data processing arrangement of claim 18, wherein the first set of coefficients results from a convolution of 3 taps of peaking filter coefficients with 4 taps of scaling filter coefficients.

20. The pixel-data processing arrangement of claim 14, wherein the vertical processing circuit and the logic circuit are implemented using a programmed processor.

21. The pixel-data processing circuit of claim 14, wherein the logic circuit is implemented using a programmed processor.